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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/924,185	HOLTZMAN ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-12,15-25,37-50,54,55,63 and 64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-12,15-25,37-50,54,55,63 and 64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20050824*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 3, 8, 10, 11, 12, 15, 16, 23, 25, 27, 28, 32, 33, and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,923,884 to Peyret et al. ("Peyret").

3. In reference to Claim 3, Peyret discloses an add-on card (See Figure 1 Number 20) for detachably coupling to a processing system (See Figure 4) comprising: an interface for communicating with said processing system while said add-on card is coupled with said processing system (See Figure 4 Number 86); a program storage memory storing at least one operating sequence (See Figure 1 Number 26 and Column 4 Line 67 - Column 5 Line 2); a mass storage memory including a program memory portion storing at least one additional operating sequence (See Figure 1 Number 30 and Column 5 Lines 7-11); and a processing unit coupled to said interface, said program storage memory, and said mass storage memory, whereby the processing unit can

operate on data transferred between the card and the processing system through the interface according to said at least one additional operating sequence (See Figures 1 and 4 Number 22 and Column 5 Lines 13-35); a card bus whereby the processing unit, the interface and the program storage memory are connected (See Figure 1); and a mass storage interface by which the mass storage memory is connected to the card bus (See Figure 1). Peyret further discloses that the mass storage is a flash memory (See Column 4 Lines 63-67) which is a type of non-linear memory, and thus, the mass storage interface is inherently a non-linear interface.

4. In reference to Claim 8, Peyret discloses the limitations as applied to Claim 3 above. Peyret further discloses that at least one additional operating sequence includes a data encryption/decryption routine (See Column 5 Lines 27-34).

5. In reference to Claim 10, Peyret discloses the limitations as applied to Claim 3 above. Peyret further discloses that the mass storage memory is a flash memory (See Column 4 Lines 63-67).

6. In reference to Claim 11, Peyret discloses the limitations as applied to Claim 3 above. Peyret further discloses that the mass storage memory further includes a portion storing system data, whereby the processing unit can operate on data transferred between the card and the processing system using the system data (See Column 5 Lines 7-11 and Column 5 Line 36 - Column 6 Line 65).

7. In reference to Claim 12, Peyret discloses the limitations as applied to Claim 3 above. Peyret further discloses that the mass storage further includes a portion for storing user data (See Column 7 Lines 33-67).

8. In reference to Claim 15, Peyret discloses: an add-on card (See Figure 1 Number 20) for detachably coupling to a processing system (See Figure 4) comprising: an interface for communicating with said processing system while said add-on card is coupled with said processing system (See Figure 4 Number 86); a program storage memory storing an operating sequence (See Figure 1 Number 26 and Column 4 Line 67 - Column 5 Line 2); a processing unit coupled to said interface and said program storage memory (See Figures 1 and 4 Number 22)., and a mass storage memory coupled to said processing unit, whereby the processor can operate on data transferred between the interface and the mass storage memory according to said operating sequence (See Figures 1 and 4 Number 30 and Column 5 Lines 13-35); a card bus whereby the processing unit, the interface and the program storage memory are connected (See Figure 1); and a mass storage interface by which the mass storage memory is connected to the card bus (See Figure 1). Peyret further discloses that the mass storage is a flash memory (See Column 4 Lines 63-67) which is a type of non-linear memory, and thus, the mass storage interface is inherently a non-linear interface.

9. In reference to Claim 16, Peyret discloses the limitations as applied to Claim 15 above. Peyret further discloses that the mass storage memory includes a program memory portion storing at least one additional operating sequence (See Figure 1 Number 30 and Column 5 Lines 7-11).

10. In reference to Claim 23, Peyret discloses the limitations as applied to Claim 15 above. Peyret further discloses that at least one operating sequence includes a data encryption/decryption routine (See Column 5 Lines 27-34).

11. In reference to Claim 25, Peyret discloses the limitations as applied to Claim 13 above. Peyret further discloses that the mass storage memory is a flash memory (See Column 4 Lines 63-67).

12. In reference to Claim 33, Peyret discloses providing an add-on card with a processing unit (See Figure 4 Number 22) and a non volatile mass storage memory (See Figure 4 Number 30), wherein a plurality of applications are stored on the add-on card, with one or more of said applications stored in the non-volatile mass storage memory (See Figure 4 Numbers 58, 62, 66, 94, and 96); causing the add-on card to be attached to the host system (See Column 7 Lines 40-42); causing the selection of an application from the plurality of applications (See Column 4 Lines 4-16); processing data stored in the mass storage memory with the processing unit, wherein said processing is performed according to the selected application (See Column 5 Lines 13-58 and

Column 6 Lines 18-20); and supplying the processed data to the host (See Column 1 Lines 9-32 and Column 5 Lines 18-35).

13. In reference to Claim 27, Peyret discloses the limitations as applied to Claim 33 above. Peyret further discloses that the processing is performed according to an application that the host lacks (See Column 1 Lines 9-32).

14. In reference to Claim 28, Peyret discloses the limitations as applied to Claim 33 above. Peyret further discloses that data stored in the mass storage memory is recorded prior to causing the add-on card to be attached to the host system (See Column 5 Lines 7-12 and Column 6 Lines 28-44).

15. In reference to Claim 32, Peyret discloses the limitations as applied to Claim 33 above. Peyret further discloses that the data is stored in the mass storage memory in encrypted form, and the processing is decrypting (See Column 5 Lines 27-34).

16. In reference to Claim 34, Peyret discloses the limitations as applied to Claim 33 above. Peyret further downloading an application from the host to the add-on card subsequent to said causing the add-on card to be attached to the host system, wherein said processing is performed according to the downloaded application (See Column 5 Lines 13-58, Column 6 Lines 18-20, and Column 7 Lines 57-67).

17. In reference to Claim 35, Peyret discloses the limitations as applied to Claim 33 above. Depew further teaches that subsequent to causing the add-on card to be attached to the host system and prior to processing data stored in the mass storage memory with the processing unit: providing data from the host to the add-on card; processing the data provided from the host with the processing unit; and storing in the mass storage memory the data from the host processed with the processing unit (See Figure 4 Number 62 and Column 7 Lines 57-67).

18. In reference to Claim 41, Peyret discloses providing an add-on card with a processing unit (See Figure 4 Number 22) and a non volatile mass storage memory (See Figure 4 Number 30), wherein a plurality of applications are stored on the add-on card, with one or more of said applications stored in the non-volatile mass storage memory (See Figure 4 Numbers 58, 62, 66, 94, and 96); causing the add-on card to be attached to the host system (See Column 7 Lines 40-42); causing the selection of an application from the plurality of applications (See Column 4 Lines 4-16); supplying data from the host to the add-on card (See Figure 4 Number 62 and Column 7 Lines 57-67); processing data supplied from the host with the processing unit, wherein said processing is performed according to the selected application (See Column 5 Lines 13-58 and Column 6 Lines 18-20); and storing the processed data in the mass storage memory (See Figure 4 Number 62 and Column 7 Lines 57-67).

19. In reference to Claim 37, Peyret discloses the limitations as applied to Claim 41 above. Peyret further discloses that the processing is performed according to an application that the host lacks (See Column 1 Lines 9-32).

20. In reference to Claim 40, Peyret discloses the limitations as applied to Claim 41 above. Peyret further discloses that the data is stored in the mass storage memory in encrypted form, and the processing is decrypting (See Column 5 Lines 27-34).

21. In reference to Claim 42, Peyret discloses the limitations as applied to Claim 41 above. Peyret further downloading an application from the host to the add-on card subsequent to said causing the add-on card to be attached to the host system, wherein said processing is performed according to the downloaded application (See Column 5 Lines 13-58, Column 6 Lines 18-20, and Column 7 Lines 57-67).

22. In reference to Claim 63, Peyret discloses the limitations as applied to Claim 33 above. Peyret further discloses that the mass storage is a flash memory (See Column 4 Lines 63-67) which is a type of non-linear memory, and thus, the mass storage interface is inherently a non-linear interface.

23. In reference to Claim 64, Peyret discloses the limitations as applied to Claim 41 above. Peyret further discloses that the mass storage is a flash memory (See Column 4

Lines 63-67) which is a type of non-linear memory, and thus, the mass storage interface is inherently a non-linear interface.

24. Claims 4, 17, 19, 29, and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Peyret and The Free On-Line Dictionary of Computing ("FOLDOC").

25. In reference to Claim 4, Peyret discloses the limitations as applied to Claim 3 above. The data transferred between the host and the add on card is inherently sent in a continuous (streaming) fashion, as evidenced by FOLDOC, which defines a stream as any flow of data from a sender to a single receiver (See 'stream').

26. In reference to Claim 17, Peyret discloses the limitations as applied to Claim 13 above. The data transferred between the host and the add on card is inherently sent in a continuous (streaming) fashion, as evidenced by FOLDOC, which defines a stream as any flow of data from a sender to a single receiver (See 'stream').

27. In reference to Claim 19, Peyret and FOLDOC disclose the limitations as applied to Claim 17 above. Peyret further discloses that the mass-storage memory contains media prerecorded by the card supplier (See Column 5 Lines 7-12 and Column 6 Lines 28-44).

28. In reference to Claim 29, Peyret discloses the limitations as applied to Claim 33 above. The data transferred between the host and the add on card is inherently sent in a continuous (streaming) fashion, as evidenced by FOLDOC, which defines a stream as any flow of data from a sender to a single receiver (See 'stream'), and thus the data stored in the mass storage memory is streamable and continuous.

29. In reference to Claim 38, Peyret discloses the limitations as applied to Claim 41 above. The data transferred between the host and the add on card is inherently sent in a continuous (streaming) fashion, as evidenced by FOLDOC, which defines a stream as any flow of data from a sender to a single receiver (See 'stream'), and thus the data stored in the mass storage memory is streamable and continuous.

30. Claim 43 is rejected under 35 U.S.C. 102(b) as being anticipated by 6,038,551 to Barlow et al. ("Barlow").

31. In reference to Claim 43, Barlow discloses providing an add-on card (See Figure 3) including a processing unit (See Figure 3 Number 50) and a non-volatile mass storage memory (See Figure 3 Number 54), wherein the mass storage memory includes a program memory portion in which are stored a plurality of applications (See Figure 3 Number 66, Column 5 Lines 7-10, and Column 11 Lines 49-65); coupling the add-on card to the host system (See Column 9 Lines 26-37); causing one of the applications to be selected (See Column 11 Lines 49-65 and Column 12 Lines 31-33); receiving data

from the host on the add-on card (See Column 11 Lines 54-65); processing data received from the host with the processing unit according to the selected application (See Column 12 Lines 31-35); and supplying the processed data to host (See Column 11 Lines 54-65).

32. In reference to Claim 44, Barlow discloses the limitations as applied to Claim 43 above. Barlow further discloses that the selected application is an application which the host lacks (See Column 5 Lines 4-11).

33. In reference to Claim 45, Barlow discloses the limitations as applied to Claim 43 above. Barlow further discloses that the data received from the host is continuous media (See Column 16 Lines 63-66).

34. In reference to Claim 48, Barlow discloses the limitations as applied to Claim 43 above. Barlow further discloses that the selected application is decryption (See Column 11 Lines 49-53).

35. In reference to Claim 49, Barlow discloses the limitations as applied to Claim 43 above. Barlow further discloses that the selected application is encryption (See Column 11 Lines 49-53).

36. Claims 54 and 55 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 6,047,342 to Depew et al. ("Depew").

37. In reference to Claim 54, Depew discloses providing an add-on card (See Figure 4 Number 340) with a processing unit (See Figure 4 Number 350), wherein a plurality of applications are stored in the combined host/card system (See Figure 3); coupling the add-on card to the host system (See Column 1 Lines 44-50); causing one of the applications to be selected (See Column 6 Lines 20-37); processing data according to the selected application, wherein said processing is performed by the card's processing unit and the host processing system together on an application level (See Column 6 Lines 30-37 and Column 7 Lines 43-54).

38. In reference to Claim 55, Depew discloses the limitations as applied to Claim 54 above. Depew further discloses that said processing comprises executing a plurality of tasks, and wherein at least one of the tasks is executed by the host processing system and at least one of the tasks is allocated by the host to be executed by the card's processing unit (See Column 6 Lines 20-29).

39. Claims 31 and 33 are rejected under 35 U.S.C. 102(b) as being unpatentable over US Patent Number 5,995,018 to Hane et al. ("Hane").

40. In reference to Claim 33, Hane discloses operating a host system to which an add-on card can be detachably coupled (See Figure 1 Numbers 2 and 3); providing an add-on card (See Figure 1 Number 1) with a processing unit (See Figure 1 Number 10) and a non volatile mass storage memory (See Figure 1 Number 11), wherein a plurality of applications are stored on the add-on card (See Column 5 Lines 1-7), with one or more of said applications stored in the non-volatile mass storage memory (See Column 5 Lines 1-7); causing the add-on card to be attached to the host system (See Column 5 Lines 8-14); causing the selection of an application from the plurality of applications (See Column 5 Lines 15-49); processing data stored in the mass storage memory with the processing unit, wherein said processing is performed according to the selected application; and supplying the processed data to the host (See Column 5 Lines 17-18).

41. In reference to Claim 31, Hane discloses the limitations as applied to Claim 33 above. Hane further discloses that the data transferred between the interface and the mass storage memory is a navigation database (See Column 8 Lines 35-60).

42. Claims 33, 41, 43, and 50 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,987,155 to Dunn et al. ("Dunn").

43. In reference to Claim 33, Dunn discloses providing an add-on card (See Figure 2 Number 25) with a processing unit (See Column 3 Lines 22-28) and a non volatile mass storage memory (See Column 3 Lines 22-28), wherein a plurality of applications are

stored on the add-on card (See Column 7 Lines 47-48 and Column 8 Line 67 – Column 9 Line 4), with one or more of said applications stored in the non-volatile mass storage memory (See Column 3 Lines 22-28); causing the add-on card to be attached to the host system (See Figure 3); causing the selection of an application from the plurality of applications (See Column 7 Lines 33-50); processing data stored in the mass storage memory with the processing unit, wherein said processing is performed according to the selected application (See Column 7 Lines 33-50); and supplying the processed data to the host (See Column 7 Lines 33-38).

44. In reference to Claim 41, Dunn discloses providing an add-on card (See Figure 2 Number 25) with a processing unit (See Column 3 Lines 22-28) and a non volatile mass storage memory (See Column 3 Lines 22-28), wherein a plurality of applications are stored on the add-on card (See Column 7 Lines 47-48 and Column 8 Line 67 – Column 9 Line 4), with one or more of said applications stored in the non-volatile mass storage memory (See Column 3 Lines 22-28); causing the add-on card to be attached to the host system (See Figure 3); causing the selection of an application from the plurality of applications (See Column 7 Lines 33-50); supplying data from the host to the add-on card (See Column 7 Lines 30-33); processing data supplied from the host with the processing unit, wherein said processing is performed according to the selected application (See Column 7 Lines 33-50); and storing the processed data in the mass storage memory (See Column 9 Lines 8-9).

45. In reference to Claim 43, Dunn discloses providing an add-on card (See Figure 2 Number 25) including a processing unit and a non-volatile mass storage memory (See Column 3 Lines 22-28), wherein the mass storage memory includes a program memory portion (See Column 3 Lines 22-28) in which are stored a plurality of applications (Column 7 Lines 47-48 and Column 8 Line 67 – Column 9 Line 4); coupling the add-on card to the host system (See Column 7 Lines 27-29); causing one of the applications to be selected (See Column 7 Lines 33-50); receiving data from the host on the add-on card (See Column 7 Lines 30-33); processing data received from the host with the processing unit according to the selected application (See Column 7 Lines 33-50); and supplying the processed data to host (See Column 7 Lines 33-38).

46. In reference to Claim 50, Dunn discloses the limitations as applied to Claim 43 above. Dunn further discloses that the selected application is voice recognition (See Column 6 Lines 8-40).

Claim Rejections - 35 USC § 103

47. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

48. Claims 5 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peyret and FOLDOC as applied to Claims 4 and 17 above, and further in view of US Patent Number 5,737,582 to Fukuzumi ("Fukuzumi-582").

49. In reference to Claim 5, Peyret and FOLDOC teach the limitations as applied to Claim 4 above. Peyret and FOLDOC do not teach a data cache memory connected to the processor and the mass storage memory for buffering the continuous media transferred between the card and the processing system. Fukuzumi-582 teaches an input/output buffer memory on an IC card for buffering data transmitted between a host device and a device on the card (See Column 14 Lines 3-6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Peyret and FOLDOC using the buffer of Fukuzumi-582, resulting in the invention of Claim 5, in order to allow a correction of any delay of the communication rate taking place between the host system and the connected device, and thus allow the host system and the device to operate at different speeds (See Column 14 Lines 3-6).

50. In reference to Claim 18, Peyret and FOLDOC teach the limitations as applied to Claim 17 above. Peyret further discloses that the mass storage is a flash memory (See Column 4 Lines 63-67) which is a non-linear memory. Thus, data is inherently stored non-linearly. Peyret and FOLDOC do not teach a data cache memory connected to the processor and the mass storage memory for buffering the data transferred between the

interface and the mass storage memory. Fukuzumi-582 teaches an input/output buffer memory on an IC card for buffering data transmitted between a host device and a device on the card (See Column 14 Lines 3-6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Peyret and FOLDOC using the buffer of Fukuzumi-582, resulting in the invention of Claim 18, in order to allow a correction of any delay of the communication rate taking place between the host system and the connected device, and thus allow the host system and the device to operate at different speeds (See Column 14 Lines 3-6).

51. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peyret as applied to Claim 3 above, and further in view of US Patent Number 6,266,671 to Niimura ("Niimura").

52. In reference to Claim 6, Peyret teaches the limitations as applied to Claim 3 above. Peyret does not teach that said at least one additional operation sequence includes a decompression program. Niimura teaches a PC card memory device which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Peyret and FOLDOC with the data

compression and decompression ability of Niimura, resulting in the invention of Claim 6, in order to increase the storage capacity of the memory and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

53. In reference to Claim 7, Peyret teach the limitations as applied to Claim 3 above. Peyret does not teach that said at least one operation sequence includes a compression program. Niimura teaches a PC card memory device which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Peyret with the data compression and decompression ability of Niimura, resulting in the invention of Claim 7, in order to increase the storage capacity of the memory and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

54. Claims 9 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peyret as applied to Claims 3 and 15 above, and further in view of Dunn.

55. In reference to Claim 9, Peyret teaches the limitations as applied to Claim 3 above. Peyret does not teach that at least one additional operating sequence includes

a voice-recognition program. Dunn teaches a smart card which receives voice recognition information from the host for processing (See Column 6 Lines 8-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Peyret with the voice-recognition processing of Dunn, resulting in the invention of Claim 9, in order to improve overall security by limiting accessibility to secure information and security processes (See Column 5 Lines 39-42).

56. In reference to Claim 24, Peyret teaches the limitations as applied to Claim 15 above. Peyret does not teach that said at least one operating sequence includes a voice-recognition program. Dunn teaches a smart card which receives voice recognition information from the host for processing (See Column 6 Lines 8-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Peyret with the voice-recognition processing of Dunn, resulting in the invention of Claim 24, in order to improve overall security by limiting accessibility to secure information and security processes (See Column 5 Lines 39-42).

57. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peyret and FOLDOC as applied to Claim 17 above, and further in view of Niimura.

58. In reference to Claim 20, Peyret and FOLDOC teach the limitations as applied to Claim 17 above. Peyret and FOLDOC do not teach that said at least one operation sequence includes a decompression program. Niimura teaches a PC card memory device which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Peyret and FOLDOC with the data compression and decompression ability of Niimura, resulting in the invention of Claim 20, in order to increase the storage capacity of the memory and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

59. In reference to Claim 21, Peyret and FOLDOC teach the limitations as applied to Claim 17 above. Peyret and FOLDOC do not teach that said at least one operation sequence includes a compression program. Niimura teaches a PC card memory device which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Peyret and FOLDOC with the data compression and decompression ability of Niimura, resulting in the invention of Claim

21, in order to increase the storage capacity of the memory and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

60. Claims 15 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hane and FOLDOC.

61. In reference to Claim 15, Hane teaches an add-on card (See Figure 1 Number 1) for detachably coupling to a processing system (See Figure 1 Number 2) comprising: an interface for communicating with said processing system while said add-on card is coupled with said processing system (See Figure 1 Number 8); a processing unit which includes a program storage memory storing an operating sequence (See Figure 1 Numbers 10 and 11); and a mass storage memory coupled to said processing unit (See Figure 1 Number 11), whereby the processor can operate on data transferred between the interface and the mass storage memory according to said operating sequence (See Column 3 Lines 32-33); a card bus whereby the processing unit, the interface, and the program storage memory are connected (See Figure 1); and a mass storage interface by which the mass storage memory is connected to the card bus (See Figure 1). Hane does not teach that the mass storage interface is a non-linear interface. Hane does teach that the memory is an EEPROM (See Column 3 Lines 19-22). FOLDOC teaches the use of Flash EPROM memory (See entry 'Flash Erasable Programmable Read-Only Memory').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hane with the Flash memory of FOLDOC, resulting in the invention of Claim 15, because Flash allows reprogramming with the chip installed (See entry 'Flash Erasable Programmable Read-Only Memory' in FOLDOC).

62. In reference to Claim 22, Hane and FOLDOC teach the limitations as applied to Claim 15 above. Hane further teaches that the data transferred between the interface and the mass storage memory is a navigation database (See Column 8 Lines 35-60).

63. Claims 30 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peyret and FOLDOC as applied to Claims 29 and 38 above, and further in view of Niimura.

64. In reference to Claim 30, Peyret and FOLDOC teaches the limitations as applied to Claim 29 above. Peyret and FOLDOC do not teach that the data stored in the memory is stored in compressed form, and the processing is decompressing. Niimura teaches a PC card memory device which is capable of decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the PC card of Peyret and FOLDOC with the data

compression and decompression ability of Niimura, resulting in the invention of Claim 30, in order to increase the storage capacity of the memory card and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

65. In reference to Claim 39, Peyret and FOLDOC teaches the limitations as applied to Claim 38 above. Peyret and FOLDOC do not teach that the selected application is data compression. Niimura teaches a PC card memory device which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the PC card of Peyret and FOLDOC with the data compression and decompression ability of Niimura, resulting in the invention of Claim 39, in order to increase the storage capacity of the memory card and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

66. Claims 46 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barlow as applied to Claim 45 above, and further in view of Niimura.

67. In reference to Claim 46, Barlow teaches the limitations as applied to Claim 45 above. Barlow does not teach that said at least one additional operation sequence includes a decompression program. Niimura teaches a PC card memory device which

is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Barlow with the data compression and decompression ability of Niimura, resulting in the invention of Claim 46, in order to increase the storage capacity of the memory and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

68. In reference to Claim 47, Barlow teaches the limitations as applied to Claim 45 above. Barlow does not teach that said at least one additional operation sequence includes a decompression program. Niimura teaches a PC card memory device which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Barlow with the data compression and decompression ability of Niimura, resulting in the invention of Claim 47, in order to increase the storage capacity of the memory and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

69. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barlow as applied to Claim 43 above, and further in view of Dunn.

70. In reference to Claim 50, Barlow teaches the limitations as applied to Claim 43 above. Barlow does not teach that at least one additionally operating sequence includes a voice-recognition program. Dunn teaches a smart card which receives voice recognition information from the host for processing (See Column 6 Lines 8-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Barlow with the voice-recognition processing of Dunn, resulting in the invention of Claim 50, in order to improve overall security by limiting accessibility to secure information and security processes.

Claim Objections

71. Claims 3-12, 15-25, 27-35, and 37-50 objected to because of the following informalities: The claims all recite the limitation of "a mass storage memory". It is unclear as to at what point the size of a memory becomes a mass storage memory. Appropriate correction is required.

Drawings

72. The drawings were received on 20 July 2005. These drawings are acceptable.

Response to Arguments

73. Applicant's arguments filed 14 July 2005 have been fully considered but they are not persuasive.

74. Applicant has argued that flash memory is not accessed in a non-linear manner. In response, the Examiner notes that the most common type of flash memory has an I/O interface which allows only sequential access to data, as evidenced by Wikipedia Article "Flash Memory" (See Page 2 Paragraph 5) and Embedded Control Europe Article "Flash-based storage devices replace hard disk drives" (See Page 1 Column 2 Paragraph 2). Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "non linear" in Claims 3-12, 15-25, and 63-64 is used by the claim to mean "not random", while the accepted meaning is "random" or "non sequential", as evidence by FOLDOC entry 'random-access memory'. The term is indefinite because the specification does not clearly redefine the term.

75. Applicant has argued that Peyret does not disclose that the processing unit, the interface, and the program storage memory are connected along the same bus. In response, the Examiner notes that the features upon which Applicant relies (i.e., connected along the *same* bus) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The claim limitations only require that the processing unit, the interface, and the program storage memory are connected by a bus. The claim limitations do not require that the components are directly connected, nor do they preclude the bus from being comprised of multiple sub-buses.

76. Applicant has argued that the memory of Peyret is not a "mass storage memory". In response, the Examiner notes that a flash memory is a type of mass storage memory, as evidenced by Wikipedia Article "Mass storage" (See Paragraph 1). Further It is unclear as to at what point the size of a memory becomes a mass storage memory.

77. Applicant has argued that Dunn does not teach "non volatile mass storage memory". In response, the Examiner notes that, as shown above, Dunn does teach this limitation. Further It is unclear as to at what point the size of a memory becomes a mass storage memory.

78. Applicant has argued that the functions of Dunn are all performed by the computer. In response, the Examiner notes that Dunn teaches that the functions can be performed on the card (See Column 7 Lines 47-48 and Column 8 Line 67 – Column 9 Line 3).

79. Applicant has argued that the ROM of Barlow is not a mass storage memory. In response, the Examiner notes that the claim limitations do not require that the mass storage memory is capable of storing data. The claim limitations only require that the mass storage memory include a program memory portion in which are stored a plurality of applications.

80. Applicant has argued that Barlow does not disclose storing a plurality of applications in the ROM, but only CRYPTOGRAPHIC PROGRAM. In response, the Examiner notes that the cryptographic program can perform a variety of different functions (which are equivalent to the applications), such as encryption, decryption, signing, and verification (See Column 11 Lines 49-65).

81. Applicant has argued that the application of Barlow is not lacking in the host, but rather is dependent upon the host. In response, the Examiner notes that the secure functions of Barlow cannot be performed by the host, as this would jeopardize the security of the system (See Abstract Lines 15-18, Column 4 Lines 34-49, and Column 5 Lines 4-10).

82. Applicant has argued that Depew does not teach performing processing by the card's processing unit and the host processing system together on an application level. In response, the Examiner notes that while CPU 310 does not perform a *significant* amount of processing, it still does perform a portion of the processing of the data, such as reviewing the data to intercept instructions, which is sufficient to satisfy the claim limitation of performing the processing together with the card's processing unit (See Column 6 Lines 20-29).

Conclusion

83. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

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